CLAIMS

1. A method comprising the steps of:

generating a first current signal representative of a lock condition of a phase lock loop between a clock in signal and a VCO signal;

generating a second current signal representative of a phase comparison between the clock in signal and a delay line output signal;

mixing the first current signal and the second current signal resulting in a combined current signal; and

providing the combined current signal to a bias input of the delay line to adjust the speed of at least one delay line element in the delay line thereby adjusting the relative timing position of the delay line output signal from the delay line.

2. The method of claim 1, further comprising the steps of:

weighting the first current signal by about 95%;

weighting the second current signal by about 5%; and

wherein the mixing step mixes the weighted first current signal and the weighted second current signal resulting in the combined current signal.

3. The method of claim 1, further comprising the steps of:

providing a plurality of strobe output signals from the delay line; and

adjusting the individual timing positions of each of the strobe output signals.

4. An electronic system comprising:

a first timing signal input for receiving a first electronic timing signal;

a phase lock loop, electrically coupled to the first timing signal input, and providing a phase lock output signal indicative of a lock condition of the phase lock loop and the first electronic timing signal;

a delay line comprising a clock input, a delay line output, and a delay line bias input, a bias signal provided to the delay line bias input adjusting the speed of at least one delay line element in the delay line thereby adjusting the relative position of a timing output signal at the delay line output relative to a timing input signal at the clock input into the delay line;

a bias adjust circuit comprising a first bias input and a second bias input, signals from the first and second bias inputs being mixed and electrically coupled to a bias output of the bias adjust circuit; and

a phase detector circuit comprising first and second phase detection inputs and a phase detection output, the phase detector circuit for coupling a phase compare signal from the phase detection output to the first bias input, the phase compare signal being based on the compared phase between signals at the first and second phase detection inputs, and wherein the first timing signal input and the delay line output are electrically coupled to the first and second phase detection inputs, and wherein the phase lock output signal is electrically coupled to the second bias input, the bias output of the bias adjust circuit being electrically coupled to the delay line bias input to provide a bias signal to the delay line.

5. The electronic system of claim 4, wherein the delay line further comprises strobe outputs, and wherein the electronic system further comprises a strobe position adjusting circuit that adjusts the timing position of the strobe signals from the strobe outputs.

6. The electronic system of claim 5, wherein the strobe position adjusting circuit comprises at least one current controlled buffer electrically coupled to at least one strobe output of the delay line for controlling the timing position of the strobe signals from the at least one strobe output.

7. The electronic system of claim 6, wherein the at least one current controlled buffer controllably adds timing delay to the strobe signals from the at least one strobe output.

8. The electronic system of claim 5, wherein the strobe position adjusting circuit comprises at least one controlled load device electrically coupled to at least one strobe output of the delay line for controlling the timing position of the strobe signals from the at least one strobe output.

9. The electronic system of claim 4, wherein the phase lock loop provides a phase lock output signal that comprises a first current signal, and wherein the phase compare signal comprises a second current signal, and the bias adjust circuit mixing the first current signal and the second current signal to provide the bias signal from the bias output of the bias adjust circuit to the bias input of the delay line.

10. The electronic system of claim 9, wherein the bias signal comprises a third current signal.

11. The electronic system of claim 10, wherein the bias adjust circuit comprises a first weighting factor circuit electrically coupled to the first bias input, and wherein the bias adjust circuit comprises a second weighting factor circuit electrically coupled to the second bias input, the bias adjust circuit mixing a weighted factor of the first current signal based on the first weighting factor circuit and a weighted factor of the second current signal based on the second weighting factor circuit to provide the third current signal.

12. The electronic system of claim 11, wherein the weighted factor of the first current signal is about 95% of the first current signal, and wherein the weighted factor of the second current signal is about 5% of the second current signal.

13. The electronic system of claim 4, wherein the delay line further comprises a plurality of strobe outputs, and wherein each of the plurality of strobe outputs is electrically coupled to a current controlled buffer for controlling the timing position of strobe signals from each of the plurality of strobe outputs.

14. The electronic system of claim 13, wherein the current controlled buffer coupled to each of the plurality of strobe outputs controllably adds timing delay to the strobe signals from each of the plurality of strobe outputs.

15. The electronic system of claim 4, wherein the delay line further comprises a plurality of strobe outputs, and wherein each of the plurality of strobe outputs is electrically coupled to a controlled load device for controlling the timing position of strobe signals from each of the plurality of strobe outputs.

16. An integrated circuit comprising:

a circuit supporting substrate; and

an electronic circuit coupled to the circuit supporting substrate, the electronic circuit comprising:

a first timing signal input for receiving a first electronic timing signal;

a phase lock loop, electrically coupled to the first timing signal input, and providing a phase lock output signal indicative of a lock condition of the phase lock loop and the first electronic timing signal;

a delay line comprising a clock input, a delay line output, and a delay line bias input, a bias signal provided to the delay line bias input adjusting the speed of at least one delay line element in the delay line thereby adjusting the relative position of a timing output signal at the delay line output relative to a timing input signal at the clock input into the delay line;

a bias adjust circuit comprising a first bias input and a second bias input, signals from the first and second bias inputs being mixed and electrically coupled to a bias output of the bias adjust circuit; and

a phase detector circuit comprising first and second phase detection inputs and a phase detection output, the phase detector circuit for coupling a phase compare signal from the phase detection output to the first bias input, the phase compare signal being based on the compared phase between signals at the first and second phase detection inputs, and wherein the first timing signal input and the delay line output are electrically coupled to the first and second phase detection inputs, and wherein the phase lock

output signal is electrically coupled to the second bias input, the bias output of the bias adjust circuit being electrically coupled to the delay line bias input to provide a bias signal to the delay line.

17. The integrated circuit of claim 16, wherein the delay line further comprises strobe outputs, and wherein the integrated circuit further comprises a strobe position adjusting circuit that adjusts the timing position of the strobe signals from the strobe outputs.

18. The integrated circuit of claim 17, wherein the strobe position adjusting circuit comprises at least one current controlled buffer electrically coupled to at least one strobe output of the delay line for controlling the timing position of the strobe signals from the at least one strobe output.

19. The integrated circuit of claim 18, wherein the at least one current controlled buffer controllably adds timing delay to the strobe signals from the at least one strobe output.

20. The integrated circuit of claim 17, wherein the strobe position adjusting circuit comprises at least one controlled load device electrically coupled to at least one strobe output of the delay line for controlling the timing position of the strobe signals from the at least one strobe output.

21. The integrated circuit of claim 16, wherein the phase lock loop provides a phase lock output signal that comprises a first current signal, and wherein the phase compare signal comprises a second current signal, and the bias adjust circuit mixing the first current signal and the second current signal to provide the bias signal from the bias output of the bias adjust circuit to the bias input of the delay line.

22. The integrated circuit of claim 21, wherein the bias signal comprises a third current signal.

23. The integrated circuit of claim 22, wherein the bias adjust circuit comprises a first weighting factor circuit electrically coupled to the first bias input, and wherein the bias adjust circuit comprises a second weighting factor circuit electrically coupled to the second bias input, the bias adjust circuit mixing a weighted factor of the first current signal based on the first weighting factor circuit and a weighted factor of the second current signal based on the second weighting factor circuit to provide the third current signal.

24. The integrated circuit of claim 23, wherein the weighted factor of the first current signal is about 95% of the first current signal, and wherein the weighted factor of the second current signal is about 5% of the second current signal.

25. The integrated circuit of claim 16, wherein the delay line further comprises a plurality of strobe outputs, and wherein each of the plurality of strobe outputs is electrically coupled to a current controlled buffer for controlling the timing position of strobe signals from each of the plurality of strobe outputs.

26. The integrated circuit of claim 25, wherein the current controlled buffer coupled to each of the plurality of strobe outputs controllably adds timing delay to the strobe signals from each of the plurality of strobe outputs.

27. The integrated circuit of claim 16, wherein the delay line further comprises a plurality of strobe outputs, and wherein each of the plurality of strobe outputs is electrically coupled to a controlled load device for controlling the timing position of strobe signals from each of the plurality of strobe outputs.